**Lab Experiment 5**

**Realization of Carry Skip Adder**

**5.1 Objective:** To design and simulate the carry skip adder (4-bit) in verilog and synthesize using EDA tools.

**5.2 Software tools Requirement**

Equipment’s:

Computer with Xilinx and Modelsim Software Specifications:

HP Computer P4 Processor – 2.8 GHz, 2GB RAM, 160 GB Hard Disk

Software’s: Synthesis tool: Xilinx ISE

Simulation tool: Modelsim Simulator

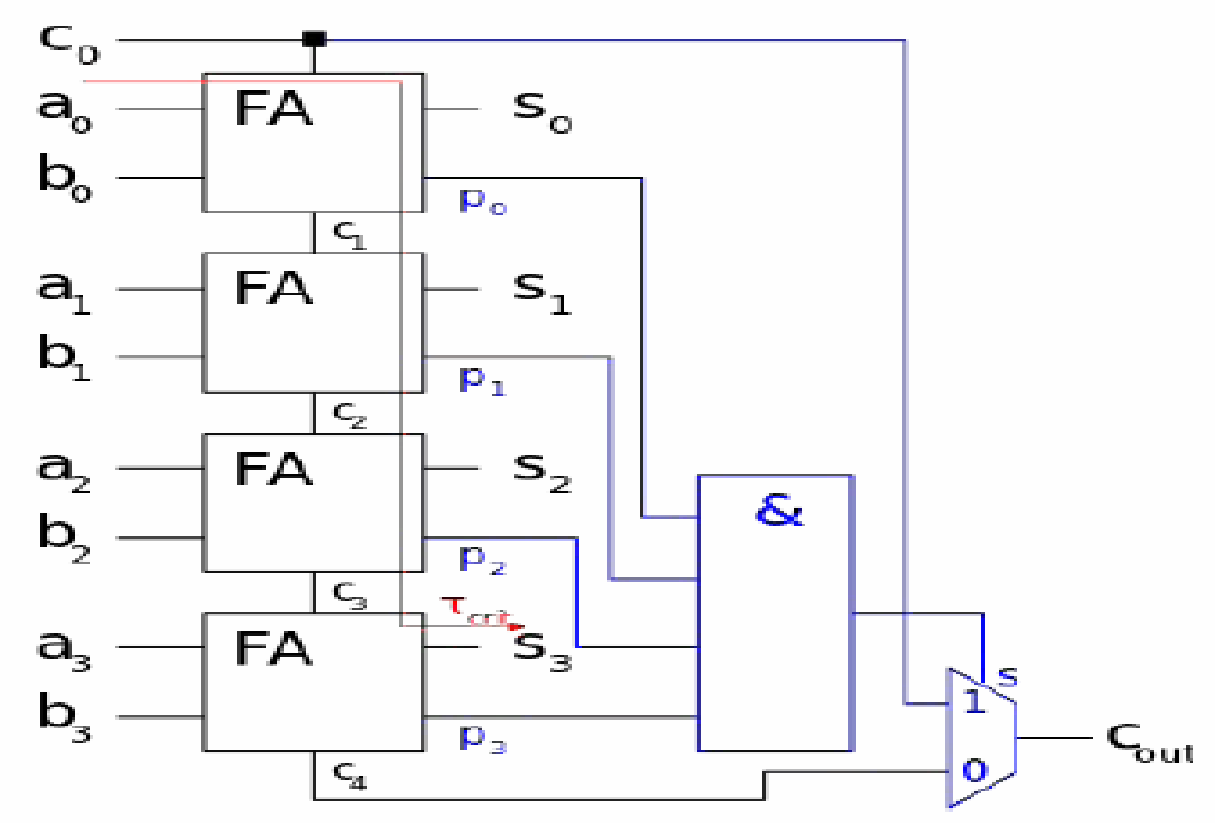
**5.3 Prelab Questions**

*(write pre lab Q & A in an A4 sheet)*

1. Write the expression for Propagate and generate term in a CLA.
2. List the efficient method for implementing 64- adder using CLA technique.

**5.4 Problem: Write a verilog code to implement the 4-bit Carry skip adder using structural model.**

**Logic Diagram:**



**Fig . 5.1 :**

**5.5 Post Lab:**

1. Compare the area, delay and power report of ripple carry & carry look-ahead adder in Xilinx ISE. Create a comparison chart and justify the results.
2. List the application of CLA in VLSI Design.
3. Prepare the synthesis Chart for a 4-bit CLA.
4. Can retiming mechanism improve the speed further in CLA architecture

**5.6 Result**

Thus, the design of 4-bit carry look-ahead adder circuit was simulated in verilog and synthesized using EDA tools.

**Lab Experiment 6**

**Realization of Multiplier-1**

**6.1 Objective:** To design and simulate the Braun array multiplier in Verilog and synthesize using EDA tools

**6.2 Software tools Requirement**

Equipment’s:

Computer with Xilinx and Modelsim Software Specifications:

HP Computer P4 Processor – 2.8 GHz, 2GB RAM, 160 GB Hard Disk

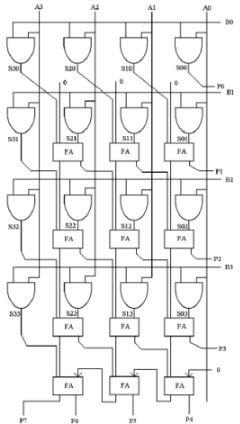
Software’s: Synthesis tool: Xilinx ISE

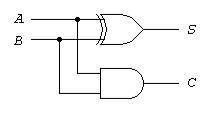
Simulation tool: Modelsim Simulator

**6.3 Prelab Questions**

*(write pre lab Q & A in an A4 sheet)*

1. What is called Booth recoding?
2. Give the booths recoding transformation of the following number 01111001(0).
3. Give the difference between Booth’s recoding and modified booth’s recoding?

**6.4 Problem: Write a Verilog code to implement the 4-bit Braun Array multipliers using structural model**

****

**LOGIC DIAGRAM**

**6.5 Post Lab:**

1. Write the booth multiplier code in Verilog and implement using EDA tools.

**6.6 Result**

Thus, the design of 4-bit Braun array multiplier circuit was simulated in verilog and synthesized using EDA tools.

**Lab Experiment 7**

**Realization of Multiplier-II**

**7.1 Objective:** To design and simulate the Wallace tree multiplier in Verilog and synthesize using EDA tools

**7.2 Software tools Requirement**

Equipment’s:

Computer with Xilinx and Modelsim Software Specifications:

HP Computer P4 Processor – 2.8 GHz, 2GB RAM, 160 GB Hard Disk

Software’s: Synthesis tool: Xilinx ISE

Simulation tool: Modelsim Simulator

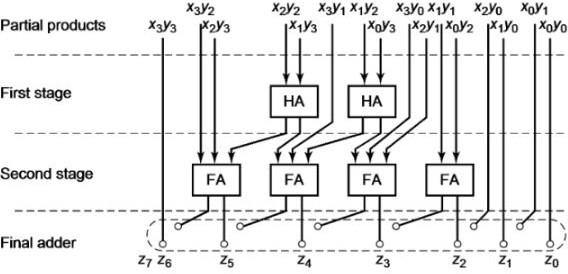
**7.3 Prelab Questions**

*(write pre lab Q & A in an A4 sheet)*

1. How carry save multiplier differs from array multiplier?
2. Why the partial sum adders are arranged in tree like fashion?

**7.4 Problem: Write a Verilog code to implement the 4-bit Wallace tree multipliers using structural model.**

**Logic Diagram:**



**Fig . 7.1 4-bit Wallace tree multiplier**

**7.5 Post Lab:**

1. Write the verilog code for 4-bit Baughly multiplier in structural modeling and implement using EDA tool.

**7.6 Result**

Thus, the design of 4-bit Wallace tree multiplier circuit was simulated in Verilog and synthesized using EDA.

# Experiment 8

# Realization of Memory

**Objective:**

Design memory using Verilog and Simulate using Xilinx Tool.

**Software tools Requirement:**

**Equipment’s:**

Computer with Xilinx and Modelsim Software Specifications.

HP Computer P4 Processor – 2.8 GHz, 2GB RAM, 160 GB Hard Disk.

**Software’s:**

Synthesis tool: Xilinx ISE.

Simulation tool: Modelsim Simulator.

**Prelab:**

1. What are the different types of memory? Compare its performance.
2. Write the difference between static and dynamic memory.
3. Define port for 32\*64k RAM memory.

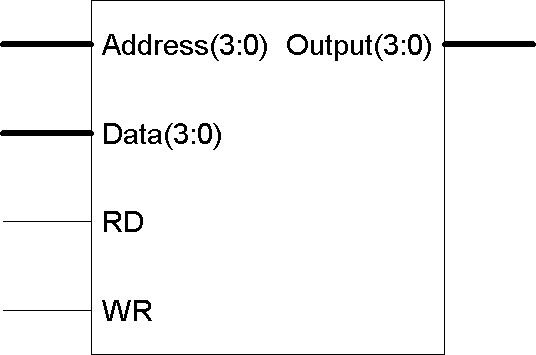
**Post Lab:**

1. Draw the block diagram and explain about FIFO memory.

**Problem Statement 1:**

1. Design 16X4 RAM Memory.

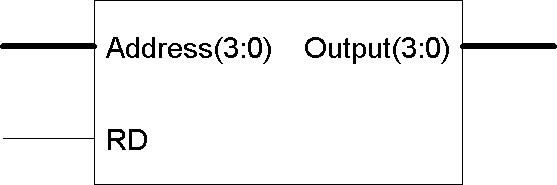
**Block Diagram:**



**Result:**

Design of a 16x8 RAM in Verilog is Performed and Verified using Xilinx Tool.

**Block Diagram:**



**Problem:** Design 16X4 ROM Memory.

**Result:** Design of a 16x4 ROM in Verilog is Performed and Verified using Xilinx Tool.

**Lab Experiment 9**

**Design and Analysis of CMOS inverter using LTSPICE**

**9.1 Objective:** To learn the design of CMOS inverter in circuit level and get the spice netlist using LTSPICE tool.

# 9.2 Software tools Requirement

Equipment’s:

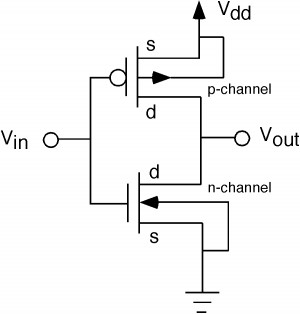
LTSPICE software

# 9.3 Prelab Questions

1. What are the advantages of SPICE software?
2. What are the differences between enhancement and depletion mode transistors?
3. What is the difference between strong 1 and weak 1?
4. What is meant by transistor sizing?

**9.4 Problem 1: Design and analyze the CMOS inverter in circuit level, verify the transfer characteristics and infer the SPICE netlist using LTSPICE.**

## 9.4.1 Logic Diagram



**9.6 Result:**

Thus, the design and analyze of CMOS Inverter has been performed, transfer characteristics have been verified using LTSPICE tool.

# Lab Experiment 10

**Design and Analysis of Complex CMOS gates and Pseudo NMOS gates using LTSPICE**

10.1 Objective: To learn the design of Complex CMOS gates and Pseudo NMOS gates in circuit level and get the spice netlist using LTSPICE tool. 9.2 Software tools Requirement

10.2 Equipment’s:

LTSPICE software

10.3 Prelab Questions

1. What is meant by Pseudo NMOS logic?
2. What are the advantages and drawbacks of Pseudo NMOS?
3. In Pseudo NMOS logic, PMOS transistor operates in resistive region.
4. What is meant by body effect?
5. What are the different types of operating region in MOSFET?

10.4 Problem 1: Design and analyze the Complex CMOS gate in circuit level, verify the transfer characteristics and infer the SPICE netlist using LTSPICE.

10.4.1 Problems:

1. complex CMOS logic for OUT= ~(A+BC)

10.5 Post lab:

1. Design Complex CMOS logic Out= ~(AB+CD) in LTSPICE.
2. Design Pseudo NMOS NAND gate in LTSPICE.

10.6 Result:

Thus, the design and analyze of Complex CMOS gate and Pseudo NMOS gate have been performed and its transfer characteristics is verified using LTSPICE.